Synopsys PathFinder-SC

Electrostatic Discharge (ESD) Integrity Analysis for Next-Generation SoC

Overview

Synopsys PathFinder-SC™ is an advanced power-noise analysis platform for system-on-chip (SoC) signoff down to 2nm. It verifies the essential protective circuitry that is present on all intellectual property (IP) and full chip SOC designs, safeguarding them from electrostatic discharge and the damage caused by voltage spikes. PathFinder-SC makes it possible for integrated circuit (IC) designers to verify and signoff even the most complex chips for ESD integrity. PathFinder-SC's cloud-optimized performance delivers 5X faster turnaround for ultra-large SoCs, which makes it ideal for today's large semiconductor designs in artificial intelligence, datacenters, imaging, networking, and 5G telecommunications.

Importance of ESD Integrity Analysis for Product Reliability

Industry surveys indicate that up to 35% of integrated circuit failures in the field are related to ESD. As silicon technology continues to shrink below 2nm, transistors become smaller and more sensitive. Guarding them against ESD and over-voltage spikes is crucial for product reliability in the field. Higher operating frequencies increased analog digital integration, and smaller product footprints only exacerbate the ESD challenge.
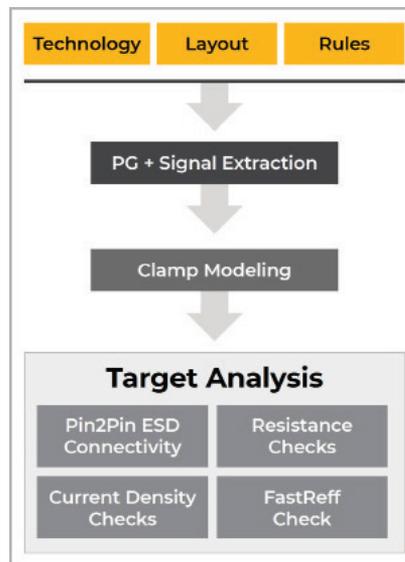

Figure 1: PathFinder-SC ESD Analysis Flow

Comprehensive ESD Coverage: HBM and CDM

PathFinder-SC can simulate events with the human body model (HBM) or the charge device model (CDM). With its comprehensive connectivity, resistance, and interconnect failure analysis, it shields every wire segment and via in the ESD discharge path.

Fast Debug with Powerful GUI and Clamp Modeling

PathFinder-SC features layout-based ESD analysis with integrated clamp modeling, extraction, and simulation engines, as well as a versatile graphical user interface (GUI) for result analysis and debugging. Along with several detailed reporting mechanisms, GUI provides visibility into ESD bus robustness and victim devices that may be impacted during ESD discharge.
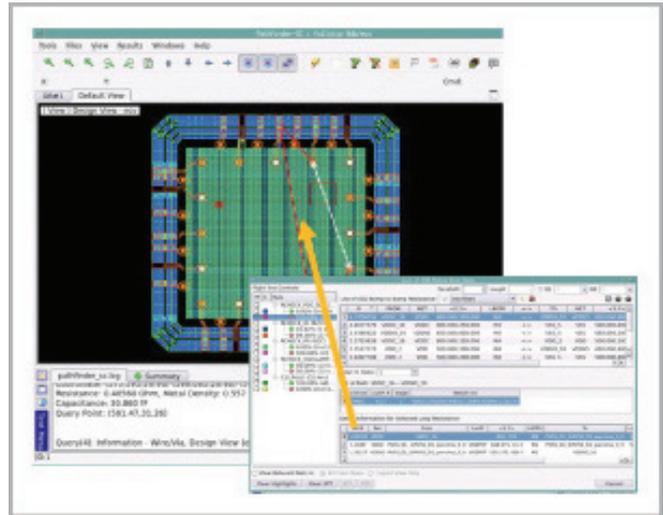

Figure 2: PathFinder-SC layout-based analysis and root cause detection

Multi-level Coverage and Hierarchical Modeling

PathFinder-SC can be used for comprehensive ESD coverage at the cell level or the IP input/output level, all the way to full-chip integration. PathFinder-SC can also write out a Compact ESD Chip Model (CECM), which is a chip-level Reduced Order Model (ROM) enabling full system-level ESD analysis.
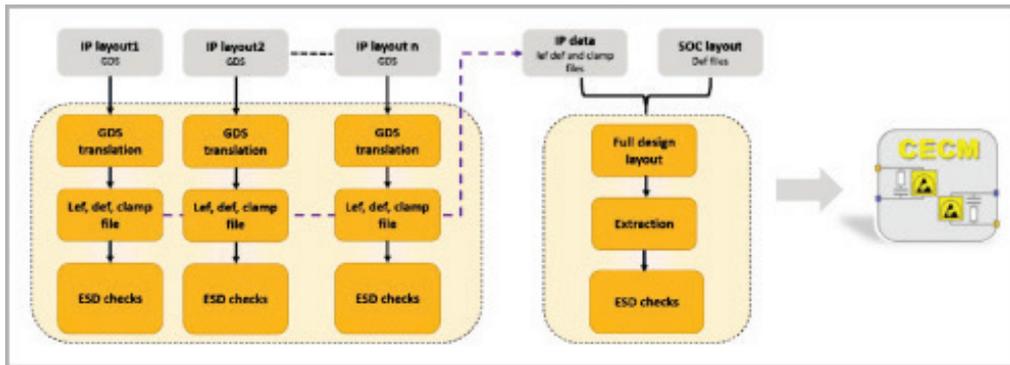

Figure 2: IP and SoC design processing flow in PathFinder-SC.
The Compact ESD Chip Model (CECM) is a reduced order model that enables full system-level ESD analysis.

Accuracy

PathFinder-SC analysis is based on foundry-certified and silicon-proven RedHawk-SC engines and has demonstrated good correlation with PathFinder.

Elastic-Compute Scalability

PathFinder-SC is a high-capacity solution built on the foundational Synopsys SeaScape™ platform – the same one used by Synopsys RedHawk-SC™ power integrity. Seascape is a big-data platform designed specifically for electronic design, engineered for elastic cloud execution across thousands of CPUs. It delivers near-linear scalability, instantaneous design bring-up and offers immense capacity while maintaining low memory per core.

PathFinder-SC has the capacity to analyze ESD integrity for SoC designs with billions of instances and deliver exceptionally fast turnaround time on commodity hardware with low memory. It accelerates proportionally as more cores become available and, unlike other tools, it doesn't require dedicated hardware, even for the largest designs, thereby decreasing overall hardware costs. The elastic scalability of PathFinder-SC has the resiliency to recover if any core or machine becomes unresponsive.
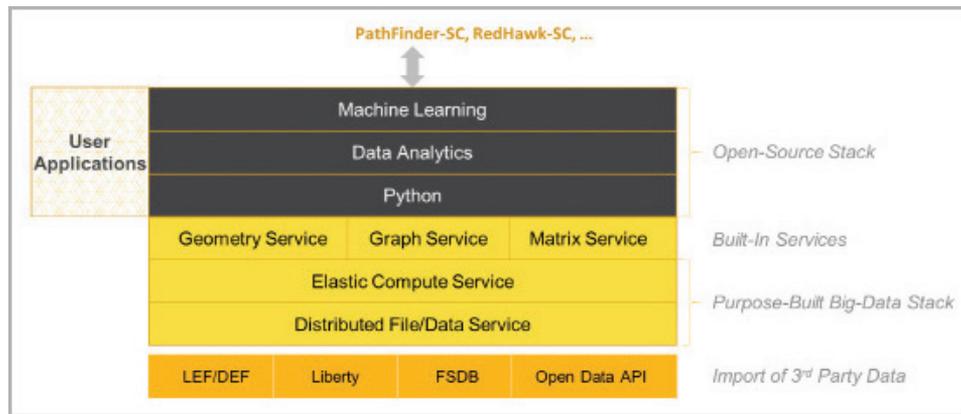

Figure 4: Cloud-optimized, Big-data SeaScape Platform for PathFinder-SC

Full-Chip Capacity

PathFinder-SC can achieve over 5x speed on large GDS processing and full-chip ESD analysis using elastic compute with commodity hardware and cloud.

Big Data Analytics

Big data analytics make it easy to do rapid data mining and analysis that can be used to drive actionable insights and optimization. Using custom data analytics, you can identify and prioritize only those design fixes that are primary to product success. Custom analytics powered by MapReduce enables you to query the largest designs in minutes.

Multi-site Collaboration Using Thin Client Support

PathFinder-SC is built for multi-site collaboration and effective design analysis. Users across multiple sites can simultaneously view, debug, and explore design and simulation results. You can load the largest designs onto small memory machines within minutes, and simultaneously view and optimize the same database across multiple sites.

Extending Coverage to 2.5D and 3D-IC Designs

2.5D/3D-IC multi-die designs have unique ESD challenges due to different IOs, die-to-die links, and technology process nodes that are significantly different from monolithic SoCs. With its elastic compute capability, PathFinder-SC can easily handle large, complex multidie architectures and ensure reliability against ESD across all levels including die, interposer, and package.

Advanced Usage Models

PathFinder-SC is customizable with user applications that can, for example, easily execute advanced full-chip CDM checks (driver receiver, clamp to instance, etc.), novel 2.5D/3D-IC ESD checks, and grid continuity checks.